PROPOSED AMENDMENTS TO THE CLAIMS:

Upon entry of this Amendment, this listing of claims will replace all prior versions and listings of claims in the application:

1-3. (cancelled)

4. (original) A variable time constant circuit using a time constant control signal, comprising:

a first signal input terminal and a second signal input terminal;

an inverting amplifier including a positive input terminal, a reverse phase input terminal, a negative output terminal, and a positive output terminal;

a first signal output terminal and a second signal output terminal which are connected to the negative output terminal and positive output terminal, respectively;

a first resistor and a second resistor which are connected in series between the first signal input terminal and the positive input terminal;

a third resistor and a fourth resistor which are connected in series between the second signal input terminal and the negative input terminal;

a first capacitor connected between the positive input terminal and the negative output terminal;

a second capacitor connected between the negative input terminal and the positive output terminal;

a first field effect transistor including a first gate terminal connected to a first junction point of the first resistor and the second resistor, a first source terminal kept at

a constant potential, and a first drain terminal connected to one of the positive input terminal and negative input terminal, the first field effect transistor flowing a current corresponding to a first voltage-current conversion ratio through the first drain terminal according to the voltage between the first gate terminal and the first source terminal;

a second field effect transistor including a second gate terminal connected to a second junction point of the third and the fourth resistor, a second source terminal kept at a constant potential, and a second drain terminal connected to the other of the positive input terminal and negative input terminal, the second field effect transistor flowing a current corresponding to a second voltage-current conversion ratio through the second drain terminal according to a voltage between the second gate terminal and the second source terminal; and

a control circuit which controls the first voltage-current conversion ratio of the first field effect transistor and the second voltage-current conversion ratio of the second field effect transistor according to the time constant control signal.

5. (original) The variable time constant circuit according to claim 4, wherein the control circuit controls a first operating point of the first gate terminal and a second operating point of the second gate terminal according to the time constant control signal.

6. (previously presented) The variable time constant circuit according to claim 4, wherein the control circuit includes a differential amplifier including a first differential input terminal pair having a first positive input terminal and a first negative

input terminal, a second differential input terminal pair having a second positive input terminal and a second negative input terminal, a first positive output terminal, and a second positive output terminal, and

the first and second positive input terminals receive the time constant signal, the first positive output terminal is connected to the first negative input terminal and to the first junction point, and the second positive output terminal is connected to the second negative input terminal and to the second junction point.

7. (previously presented) The variable time constant circuit according to claim 4, wherein the control circuit includes a first differential amplifier having a first positive input terminal, a first negative input terminal, a first positive output terminal, and a second positive output terminal, and a second differential amplifier which has a second positive input terminal, a second negative input terminal, a third positive output terminal, and a fourth positive output terminal, and

the first positive input terminal and the second positive input terminal receive the time constant control signal, the first positive output terminal and third positive output terminal are connected to the first negative input terminal and to the first junction point, and the second positive output terminal and fourth positive output terminal are connected to the second negative input terminal and to the second junction point.

8. (original) The variable time constant circuit according to claim 4, wherein the inverting amplifier includes a common-source amplifier.

9. (original) The variable time constant circuit using an operating point setting signal and according to claim 4, further comprising an operating point setting circuit which sets an operating point of each of the positive input terminal and negative input terminal of the inverting amplifier according to the operating point setting signal.

10. (previously presented) The variable time constant circuit according to claim 9, wherein the operating point setting circuit includes a differential amplifier including a first differential input terminal pair having a first positive input terminal and a first negative input terminal, a second differential input terminal pair having a second positive input terminal and a second reversed input terminal, a first positive output terminal, and a second positive output terminal, and

the first and second positive input terminals receive the time constant signal, the first positive output terminal is connected to the first negative input terminal and to the positive terminal of the inverting amplifier, and the second positive output terminal is connected to the second negative input terminal and to the negative terminal of the inverting amplifier.

11. (previously presented) The variable time constant circuit according to claim 9, wherein the operating point setting circuit includes a first differential amplifier including a first positive input terminal, a first negative input terminal, a first positive output terminal, and a second positive output terminal, and a second differential amplifier including a second positive input terminal, a second negative input terminal, a third positive output terminal, and a fourth positive output terminal, and

the first positive input terminal and the second positive input terminal receive the time constant control signal, the first positive output terminal and third positive output terminal are connected to the first negative input terminal and to the first junction point, and the second positive output terminal and fourth positive output terminal are connected to the second negative input terminal and to the second junction point.

12. (previously presented) A filter circuit comprising a plurality of unit filters connected in cascade, each of which includes a variable time constant circuit, the variable time constant circuit using a time constant control signal and comprising:

a first signal input terminal and a second signal input terminal;

an inverting amplifier including a positive input terminal, a reverse phase input terminal, a negative output terminal, and a positive output terminal;

a first signal output terminal and a second signal output terminal which are connected to the negative output terminal and positive output terminal, respectively;

a first resistor and a second resistor which are connected in series between the first signal input terminal and the positive input terminal;

a third resistor and a fourth resistor which are connected in series between the second signal input terminal and the negative input terminal;

a first capacitor connected between the positive input terminal and the negative output terminal;

a second capacitor connected between the negative input terminal and the positive output terminal;

a first field effect transistor including a first gate terminal connected to a first junction point of the first resistor and the second resistor, a first source terminal kept at a constant potential, and a first drain terminal connected to one of the positive input terminal and negative input terminal, the first field effect transistor flowing a current corresponding to a first voltage-current conversion ratio through the first drain terminal according to the voltage between the first gate terminal and the first source terminal;

a second field effect transistor including a second gate terminal connected to a second junction point of the third and the fourth resistor, a second source terminal kept at a constant potential, and a second drain terminal connected to the other of the positive input terminal and negative input terminal, the second field effect transistor flowing a current corresponding to a second voltage-current conversion ratio through the second drain terminal according to a voltage between the second gate terminal and the second source terminal; and

a control circuit which controls the first voltage-current conversion ratio of the first field effect transistor and the second voltage-current conversion ratio of the second field effect transistor according to the time constant control signal.